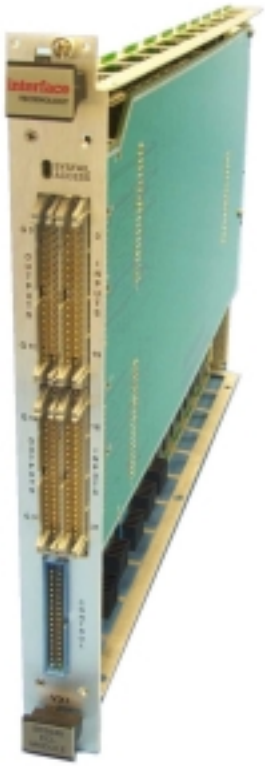

# SR5040

## *Differential ECL I/O Module For SR5000 Digital Test Subsystem*

- 32 Input and 32 Output Pins per Module
- 64K Vectors per Channel
- RAM-Backed and Algorithmic Pattern Generation
- NRZ, RZ, RONE, and RTC Output Data Formats Supported
- 16 Timing Generators per Module
- Two Response Generators per Module
- 100 ps Edge Placement Resolution

## High Channel Density

The SR5040 ECL I/O Module provides 32 stimulus pins and 32 response pins in a single C-size slot. Up to 20 I/O modules may be controlled by the SR5010 Timing/Control Module for a total of 640 I/O pins. Intermodule communication occurs through a VXI register-based interface and VXI direct memory access.

## Six Distinct I/O Memory Types

The SR5040 I/O Module contains six separate memory banks, each 64K vectors in depth, for generating stimulus patterns, expected response patterns, and recording UUT response data.

The Stimulus Memories contain the Output and Algorithmic patterns, which are used to define the stimulus output to the UUT. The Response Memories contain the Expect, Algorithmic, and Mask patterns, which are used to define the expected response from the UUT. The Mask Memory provides a means to ignore individual response data bits on a vector by vector basis. Algorithmic Memory is used to define the arithmetic operations needed to generate stimulus and response data with the algorithmic hardware.

Record Memory can be used to store either the response data or the result of the comparison between the response data and the Expect Memory. It is operated independently in a manner much like a logic analyzer. A sixteen level state machine and nine system-wide comparators are used to control what data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CCITT CRC register for signature analysis applications.

## 18 Timing Generators per Module

Each I/O module contains 18 separate timing generators for stimulus and response edge placement. Each output pin can select from 4 timing generators to define the leading and trailing edges of each stimulus pin. Each group of eight output pins share an independent set of 4 timing generators for a total of 16 stimulus timing generators per card. Each response pin can select from 2 response timing generators to define the sample and compare edges, or the 2 response timing generators can be combined together for window compare with glitch detection.

## Multiple Data Formats

Each stimulus pin may be independently programmed for any of the following formats: Non-Return to Zero (NRZ), Return to Zero (RZ), Return to One (RONE), and Return to Complement (RC).

# *SR5040 SPECIFICATIONS**

## Channels per Module:

| | |
|---|---|
| Inputs | 32 |
| Outputs | 32 |

## Memory Types:

| | |
|---|---|
| Stimulus | Output, Algorithmic |
| Response | Expect, Mask, Algorithmic |
| Record | |

## Memory Depth:

| | |
|---|---|
| Memory Depth: | 65,500 vectors |

## Output Timing:

| | |
|---|---|
| Clock Pairs (assert/deny) | 8 total per card; 2 per 8 channels |
| Delay Range | One clock period |
| Resolution | 100 ps, nonmontonic<br>2.0 ns, monotonic |
| Delay Accuracy | 2.0 ns typ., 3.0 ns maximum |
| Output Pulse Width | Min: 10 ns<br>Max: period clock - 10 ns |
| Pulse Width Accuracy | 3.0 ns typ., 5.0 ns maximum |

## Skew:

| | |
|---|---|
| Same Module | ±2 ns typical, ±4 ns maximum |
| SR5040-SR5040 | ±3 ns typical, ±5 ns maximum |

## Data Formats:

| | |
|---|---|
| RZ | Return to Zero |
| NRZ | Non-Return to Zero |
| RONE | Return to One |
| RC | Return to Complement |

## Output Drivers:

| | |
|---|---|
| Type | Differential ECL, 100324 |
| Voh (50 ohms to -2.0 V) | -1.025 V, min., -0.870 V, max. |
| Vol (50 ohms to -2.0 V) | -1.830 V, min., -1.620 V, max. |
| Output Termination | 50 ohms to -2.0 volt |

## Input Receivers:

| | |
|---|---|
| Type | Differential ECL, 100325 |
| Vih (single-ended) | -1.165 V, min., -0.870 V, max. |
| Vil (single-ended) | -1.830 V, min., -1.475 V, max. |
| Vdiff (differential) | 150 mV, min. |
| Input Termination | 50 ohms to -2.0 V |

## Input Sample / Compare Modes:

| | |
|---|---|
| Formats | Edge / window |
| Range | One period clock cycle |
| Resolution | 100 psec |
| Accuracy | ±1 ns typical; ±2 ns maximum |

## Input Timing:

| | |
|---|---|
| Sample/Compare Clocks | Two per card (edge mode);<br>One per card (window mode) |
| Input Delay Range | One clock period |
| Clock Separation | 10 ns, min. |
| Resolution | 100 ps, nonmonotonic<br>2.0 ns, monotonic |

# VXI Specifications

## Interface Compatibility:

| | |
|---|---|
| Type | Register-based, servant only<br>(controlled by SR5010) |
| Revision | 1.3 and 1.4 |
| Size | C-size, single slot |
| Configuration | Static |
| Memory | 2 MB VME A32/D32 |

## Power Requirements:

| | | |
|---|---|---|
| +5.0 volts | 9.5 A | 47.50 W |
| -5.2 volts | 4.2 A | 21.84 W |
| +12.0 volts | 0.1 A | 1.2 W |
| -12.0 volts | 0.1 A | 1.2 W |
| -2.0 volts | 2.8 A | 5.6 W |
| | | -------- |
| Total Power | | 77.34 W |

## Cooling Requirements:

| | |
|---|---|
| Per-slot Average | 78 W maximum |
| Airflow | 6 L/sec @ 0.38 mm water pressure<br>for 10°C temperature rise |

## Environmental Specifications:

| | |
|---|---|
| Temperature | Storage = -40°C to +75°C<br>Operating = 0°C to +45°C |
| Humidity | 5% to 95% relative, noncondensing |

## Software Drivers:

| | |
|---|---|
| National Instruments | LabView |
| National Instruments | LabWindows/CVI |

* Specifications subject to change without notice.

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